ABSTRACT OF THE DISCLOSURE

A level shifter 13 is provided for each of SR flip flops F1 constituting a shift register 11. The level shifter 13 increases a voltage of a clock signal CK. This arrangement reduces a distance for transmitting a clock signal whose voltage has been increased, as compared with a construction in which a voltage of a clock signal is increased by a single level shifter and the signal is transmitted to each of the flip flops; consequently, a load capacity of the level shifter can be smaller. Furthermore, each of the level shifters is operated during a pulse output of the previous level shifter 13, and the operation is suspended at the end of the pulse output. Thus, the level shifters 13 can operate only when it is necessary to apply a clock signal CK to the corresponding SR flip flop F1. As a result, even when an amplitude of a clock signal is small, it is possible to reduce power consumption of the shift resister under normal operation.